

Docket No.: 43889-937

**PATENT**

# 2  
j1040 U.S. PTO  
09/843687  
04/30/01

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of

Sadami TAKEOKA, et al.

Serial No.:

(Continuation of Serial No. 08/803,145)

Group Art Unit:

Filed: April 30, 2001

Examiner:

For: METHOD OF DESIGNING SEMICONDUCTOR INTEGRATED CIRCUIT

**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
Washington, DC 20231

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached form PTO-1449. It is respectfully requested that the references be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

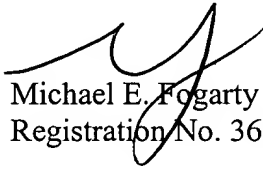
This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

(Continuation of Serial No. 08/803,145)

The references were cited by or submitted to the U.S. Patent and Trademark Office in parent application Serial No. 08/803,145, filed February 19, 1997, which is relied upon for an earlier filing date under 35 USC 120. Thus, copies of these references are not attached. 37 CFR 1.98(d).

Respectfully submitted,

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**INFORMATION DISCLOSURE  
CITATION IN AN  
APPLICATION**

(PTO-1449)

ATTY. DOCKET NO.  
**43889-937**

SERIAL NO.  
**(Continuation of Serial  
No. 08/803,145)**

APPLICANT  
**Sadami TAKEOKA, et al.**

FILING DATE  
**April 30, 2001**

GROUP

040 U.S. PTO  
09/843687  
04/30/01

**U.S. PATENT DOCUMENTS**

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	4,860,290	8/89	Daniels et al.			
	5,602,855	2/97	Lee Whetsel, Jr.			
	5,631,911	5/97	Lee Whetsel, Jr.			
	5,852,364	12/98	Lee Whetsel			
	5,884,023	3/99	Swoboda et al.			
	5,987,635	11/99	Kishi et al.			
	4,703,435	10/87	Darringer et al.			
	5,043,986	8/91	Agrawal et al.			
	5,299,136	3/94	Babakanian et al.			
	5,461,573	10/95	Chakradhar et al.			
	5,513,118	4/96	Dey et al.			
	5,550,749	8/96	Dey et al.			
	5,684,721	11/97	Swoboda et al.			
	5,761,215	6/98	McCarthy et al.			

**FOREIGN PATENT DOCUMENTS**

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
	7-271845	10/20/95	Japan				
	8-87538	2/4/96	Japan				

**OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)**

	"Partial Scan at the Register-Transfer Level", by Steenoma et al., IEEE 1993, pp. 488-497.

EXAMINER	DATE CONSIDERED
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